Car radio cluster family

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Circuit Description

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Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

Description des cicuits Schaltungsbeschreibung Kredsløbsbeskrivelse Kretsbeskrivelse Kretsbeskrivning Toimintaselostus Descrizione del circuito Descripción del circuito

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Chapter 1. Introduction of the Cluster family

The term "Cluster" is a collective name for a new series of carradios. This Cluster family has been divided in three subgroups , viz. Cluster A, Cluster A/B and Cluster B. Fig. 1.1 shows which sets belong to which subgroup. It is also possible to derive from this figure with which features a set has been equipped.
In broad outline this new family differs in two respects from the preceding family, the PLL family. The first respect is the exterior, namely the styling of the Cluster sets. The second respect concerns the interior, the technique applied for the realization of the features. This circuit description is aimed at getting insight into the newly used circuits and the associated ICs. The striving here has been to consider the most extensive set as the basis. At the time of the creation of this description cluster B sets were not yet in production and were thus not available. This is why the basis of this description is the most extensive Cluster A/B set, the 22DC685. However, this implies that some features mentioned in this description will not be dealt with. This is for instance the case with Radio Data System (RDS) and Vibration Dependent Volume Control (VDVC). But RDS is applied in a Cluster A/B set. For this purpose reference is made to the related circuit description.

Chapter 2. Block diagram

A better insight into the interrelation of the components is obtained if the whole is reduced to a block diagram. This block diagram, represented in Fig. 2.1., shows that the system makes use of an I²C bus. Striking is that all audio controls are also driven via the I²C bus by the µC (6166). The IC which translates the digital information into analogue controls is the SOFAC (Sound and Fader Control). This IC is discussed in detail in chapter 7.
Another new aspect for the Cluster family is the application of a stereo decoder and an SK decoder in thick–film technique (THI–FI). The circuits realized on the thick films do not differ principally from formerly applied ones. As to the radio section two things can be stated in the first instance.
The FM high–frequency section has been accommodated in a tuning module. The technique processed in it is partially new. In chapter 3 we will briefly deal with this module.
The second remark concerns the AM–IF section. For the Cluster family the AM–IF is 10,7 MHz, thus equalling the FM IF. This will be discussed in chapter 4.

CLUSTER FAMILY

	A						A/B					B	
	570	574	575	670	674	675	680	684	681	682	685	774	794
FM		*			*								
FM-M-L	*		*	*		*	*	*	*	*	*		
FM-M-L-S												*	*
SDK		*	*		*	*		*			*	*	*
SEC.CODE	*		*	*		*	*	*	*	*	*	*	*
AUTOST.			*			*	*	*	*	*	*	*	*
FADER							*	*	*	*	*	*	*
LOUDN.	*		*	*		*	*	*	*	*	*		
LINEOUT									*	*	*	*	*
METAL									*	*	*	*	*
DOLBY									*	*	*	*	*
VDVC													
RDS										*			
ADS													*
MSS									*	*	*		*
REM.CONT												*	
P1–8	*	*	*										
P6–16				*	*	*	*	*					
P6–17									*	*	*		
P6S–2												*	*

-- VDVC = Vibration Dependent Volume Control
-- RDS = Radio Data System
-- ADS = Antenne Diversity System

Fig. 1.1

-BLOCKDIAGRAM-

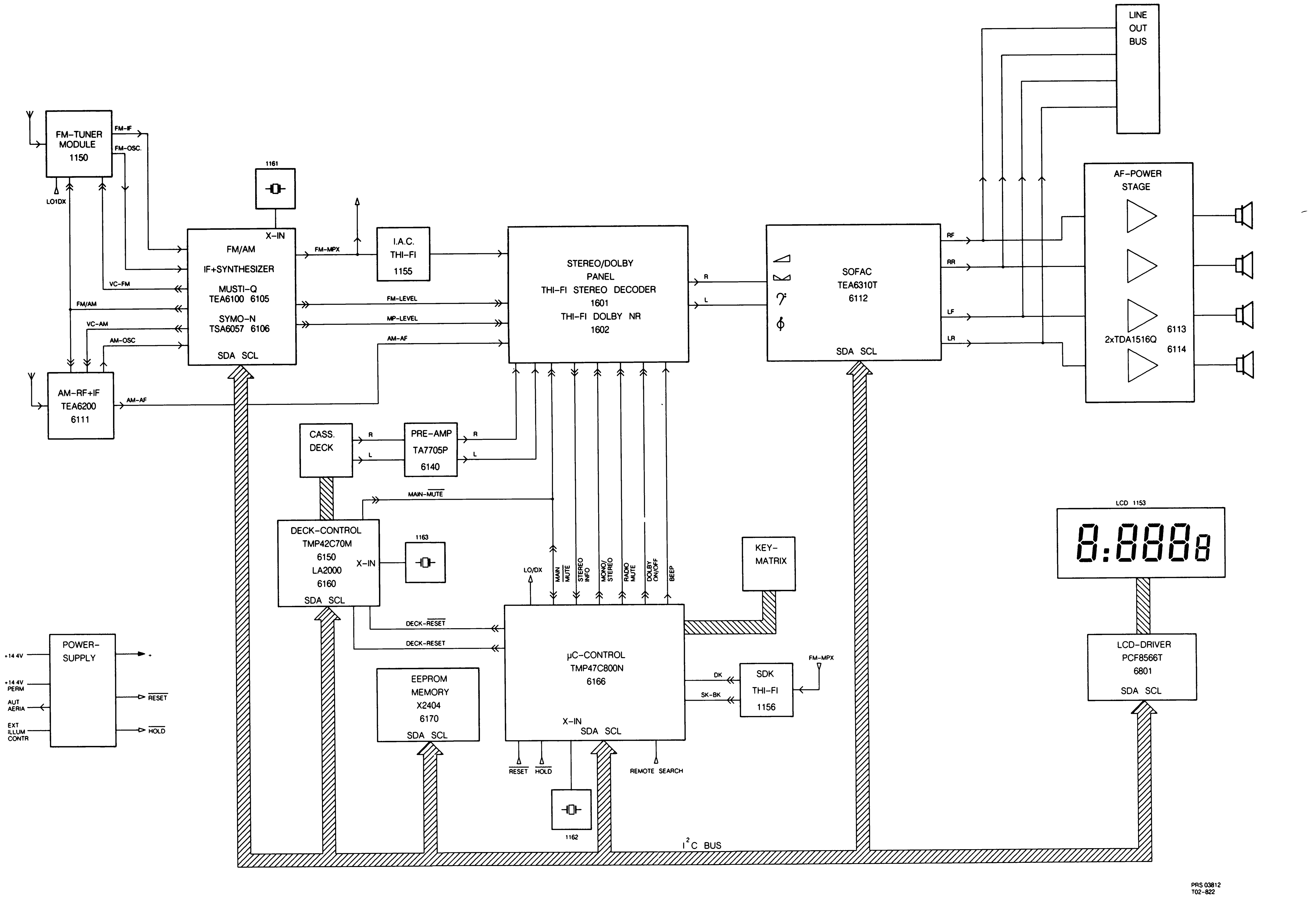

Fig.2.1

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Chapter 3. FM section

3.1. FM tuning module.

The applied tuning module has been designed especially for reception systems in carradios. The module contains an RF front-end which is tuned by means of varicap diodes, a selective IF section and an IF amplifier. The basis of this module is formed by IC U4062B. This IC sees to all the necessary functions such as the RF section, the IF section, the local oscillator, the mixer and the AGC control.
The concept of the tuning unit is such that the unit need only be adjusted once. The IF output has been designed for direct coupling with the TEA6100 (MUSTI–Q), while the oscillator output and the required tuning voltage have been adapted to the TSA6057 (SYMO–N). The amplification of the IF amplifier can be set by means of an external resistor, if necessary.
For this module the tuning voltage is lying between 1,2 V and 5,5 V and at this voltage a frequency range of 87,5 – 108 MHz can be realized. For the reduction of the reception sensitivity the tuner has been provided with an LO/DX connection. This is among other things used with the multi–level autostore feature.

3.2. FM intermediate frequency

3.2.1. General

In chapter 3.1. we have seen that from the tuning module the FM intermediate frequency is available in filtered form. The block diagram in Fig. 2.1. shows that this IF signal is fed into a block which we have called the FM/AM IF+ synthesizer. This block is in combination with the tuning module and microcomputer (6166) TMP47C800N responsible for the exact transmitter tuning. Fig. 3.1 shows the circuit diagram of the IF section. It is important now what the TEA6100 (MUSTI–Q) does and how this IC has been built up.

3.2.2. Introduction of the TEA6100 (MUSTI–Q).

The TEA6100 is an integrated FM/IF system, combined with an AM/FM tuning interface. It has been designed for microcomputer-controlled reception systems for which the internal communication takes place via an I^2C bus. The TEA6100 can be considered as the successor of the TEA6000 (MUSTI–I) which was applied in the PLL family, but in broad outline with the following major differences:

- The TEA6100 offers the possibility of being applied in systems with an AM–IF of 10,7 MHz.
- The system makes use of a quadrature demodulator with a ratio–detector–like behaviour. A major advantage here is that considerably fewer external components are required.
- The α–3dB IF limitation can also be set with a maximum spread in the FM front–end amplification of approx 10 dB.

In the following sections the TEA6100 will be discussed in detail.

3.2.3. IF system philosophy of the TEA6100.

The FM and AM reception quality of an electronically tuned receiver strongly depends on the transmitter detection circuits used. The increasing complexity of the equipment and the appearance of ever more transmitting stations are the cause for constantly higher requirements to be posed on the detection circuits for an optimal signal reception. Before that time, and even now, the following systems were used:

- AM narrow–band detector.
- FM window detector in combination with AFC (Automatic Frequency Control).

They imply a number of drawbacks, especially with respect to the AM detector which, as a result of its high selectivity, is very sensitive to frequency drift due to fluctuations in temperature. To a lesser degree this also applies to the FM detector, although the above–mentioned phenomenon is offset by the AFC. To solve these problems TEA6100 has been provided with an IF measuring system, coupled with a computer interface which puts the measured values on the I^2C bus. In this way the tuning data is available to the microcomputer. The exact tuning has been reached when the measured frequency equals the response frequency of the IF filters. TEA6100 can measure both the 10,7 MHz and the 460 kHz. The tuning accuracy now mainly depends on the accuracy of the IF measurement.

In its turn the IF measuring accuracy depends on the reference frequency used by the counter. With the Cluster family a reference frequency of 40 kHz is applied, but TEA6100 offers the possibility of using 32 kHz as reference frequency. The afore–mentioned 40 kHz is retrieved from the SYMO–N (6106), the TSA6057. The TSA6057 has a crystal–controlled internal clock, operating at a frequency of 4 MHz. Via an internal frequency divider, in this case a divider by 100, 40 kHz is presented to TEA6100 via pin 9 of TSA6057. This system gives the counter of TEA6100 an accuracy of ± 500 Hz at an AM–IF of 10,7 MHz.
Because the exact tuning information from the IF counter is via the interface continuously passed on to the microcomputer, an AFC system is not required. This offers the possibility of placing an IF soft mute (see Fig. 3.2) between the limitation amplifier and the quadrature demodulator. This soft mute stage has been equipped with a switch–on delay capacitor (2115, 2103) and is driven by a DC voltage coming from the IF level detector. This results in a ratio–detector–like behaviour, still the most desired one for carradios.
Another phenomenon that presents itself with carradio systems is multi–path distortion as a result of carrier reflection by obstacles. The presence of multi–path reception is not eliminated in TEA6100 but it is detected by the IF level detectors. The DC voltage of the internal output of the level amplifier (see Fig. 3.2) will in case of reception of a transmitter with multi–path distortion contain a superimposed AC voltage. This AC voltage is via a bandpass filter presented to a rectifier in combination with an amplifier and converted into a usable DC voltage level. This DC voltage which is a measure for the multi–path distortion can be applied for a number of purposes:

- Adaptating the frequency response with respect to the audio section. This is called SDR (Signal Dependent Response).
- Realizing in the stereo decoder a gradual transition from stereo to mono and vice versa. This is called SDS (Signal Dependent Stereo).
- Decision level for the microcomputer to ignore a transmitter during searching.

The related DC voltage is also available as digital data since this level is also via an analogue/digital converter presented to the I^2C bus.

3.2.4. Function description of the TEA6100.

In broad outline the TEA6100 can be split in two sections, the analogue signal processing section and the digital tuning interface section. The related sections will separately be studied in more detail.

3.2.4.1. Analogue signal processing section.

Fig. 3.2 shows the block diagram of the analogue section. The diagram shows that an IF signal can be presented to pins 18 and 19 of the TEA6100. These inputs can be switched on and off via the I^2C bus. To both inputs applies that they are suited for both AM and FM signals. The related IF signal is presented to a 4–stage symmetric limiting amplifier. This circuit also contains 5 IF level detectors. Later we will discuss how the IF level detection and control operates. From the afore–mentioned amplifier the signal goes via a control amplifier to the IF counter and in the FM option also to an IF mute circuit. From this mute circuit the FM–IF goes to a symmetric quadrature demodulator. The AF signal coming from the demodulator is first amplified and then presented to the output (pin 1) of the TEA6100.

– Detection of the IF level and multi–path.

The AM/FM level amplifier is driven by 5 IF level detectors. Dependent on the measured IF level the AM/FM level amplifier generates a DC voltage. This DC voltage, externally available at pin 3, does not only depend on the IF level but also on an external level adjustment by means of a DC voltage. This external adjustment is used for the α–3dB setting in the FM mode and for the search level setting in the AM mode. The IF level output (pin 3) is used internally for the mute control and is also presented to an analogue/digital converter (ADC–1) and via this converter it is applied to the I^2C bus. In most cases the voltage on the related pin will be a fluctuating DC voltage but may also contain additional data.

This is the case when multi–path reception occurs during FM reception. The degree of multi–path reception is detected by the IF level detectors and passed on to the level amplifier. Now too a multi–path reception dependent AC voltage will be superposed on the fluctuating DC voltage at the output of the level amplifier. To separate the level changes as a result of the fluctuating field strength from the level changes as a result of the multi–path reception, the signal of pin 3 is presented to a 3 kHz bandpass filter. Now the filtered signal only contains multi–path data. This data, in the form of a kind of AC voltage, is detected, rectified and amplified. Detection takes place in the multi–path detector. The detected signal is applied to the input of a TTL selector, whose output is connected with an amplifier. This amplifier serves for the amplification of the detected multi–path signal and for the amplification of AM–IF level signals. The AM–IF level signals are presented to the amplifier via the second input of the selector. By switching the TEA6100 via the I^2C bus in the AM mode the switch is actuated. Later we will discuss how the AM–IF level signals are processed. We will now continue with the detected and amplified multi–path signal. Through these operations a usable DC voltage is obtained whose level depends on the multi–path reception. This DC voltage is externally available at pin 5 and is also via an analogue/digital converter applied to the I^2C bus. In this way this data is available to the microcomputer. In this case capacitor 2113 (see Fig. 3.1) connected to pin 5 serves as buffer capacitor.

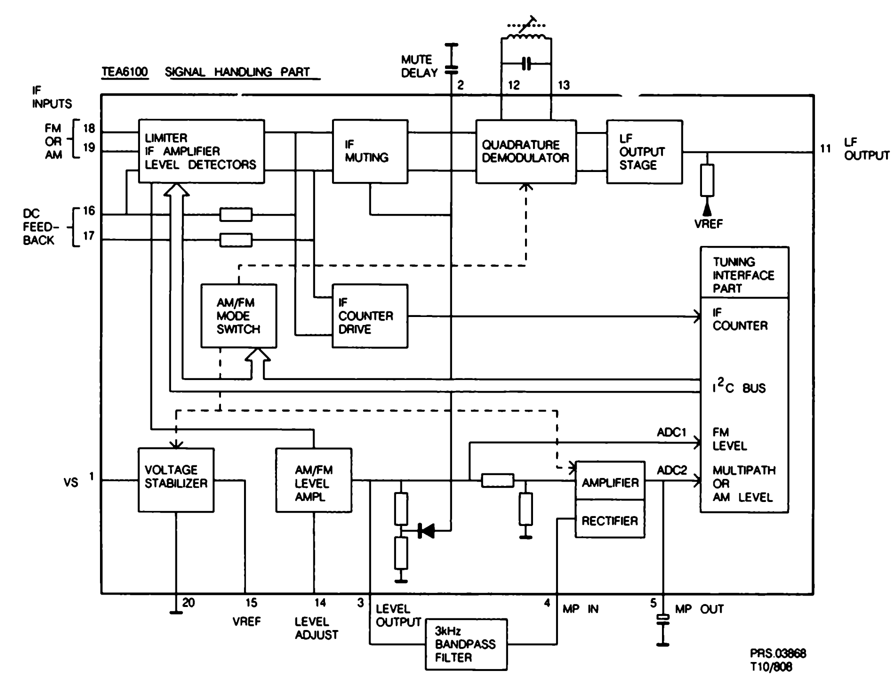
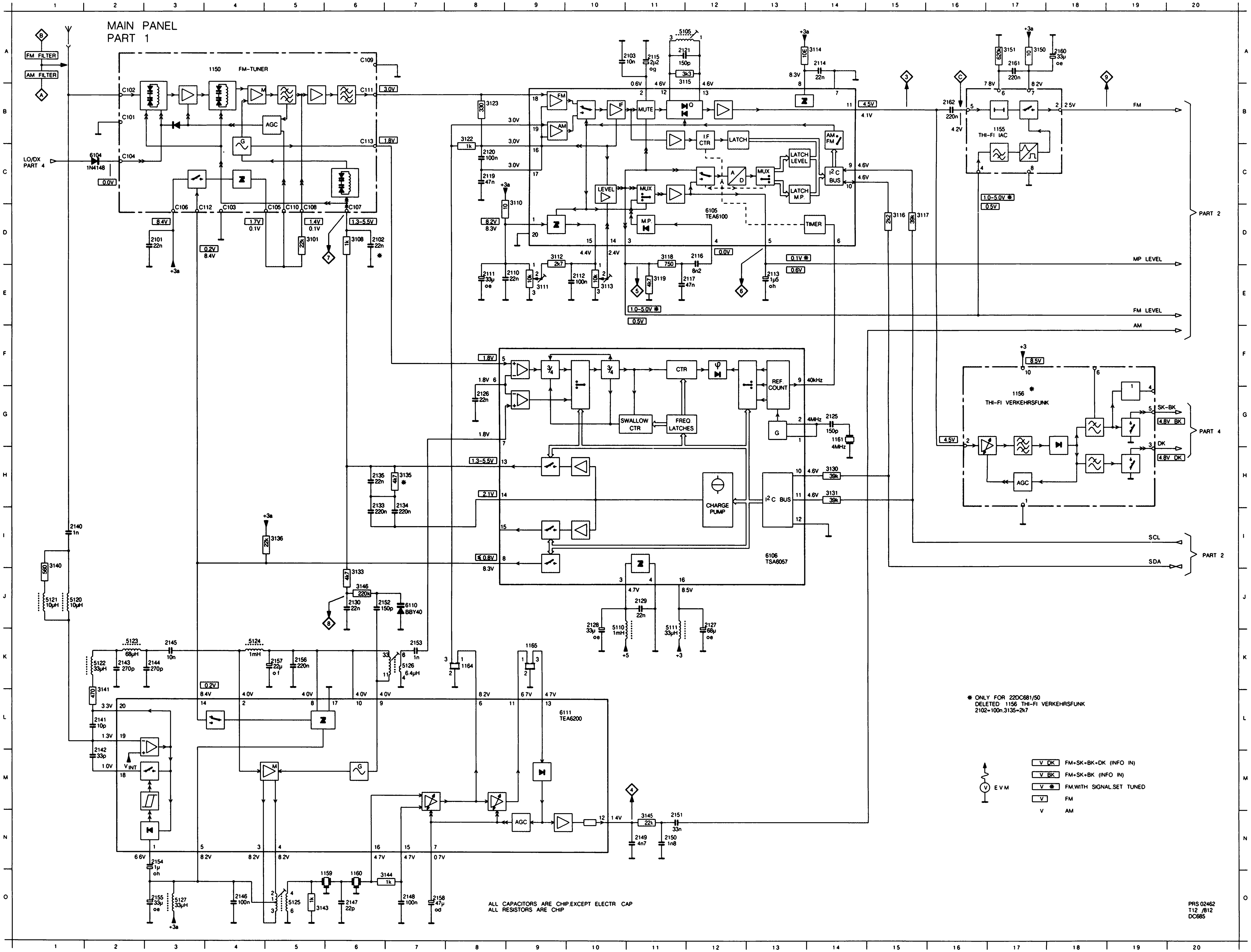


Fig.3.2



1150	A 4
1155	B17
1156	G17
1159	O 6
1160	O 6
1161	G14
1164	K 8
1165	K 9
2101	D 3
2102	D 6
2103	A11
2110	E 9
2111	E 8
2112	E10
2113	E13
2114	A14
2115	A11
2116	D12
2117	E12
2119	C 8
2120	C 8
2121	A11
2125	G14
2126	G 8
2127	J12
2128	J10
2129	J11
2130	J 6
2133	H 6
2134	H 7
2135	H 6
2140	I 1
2141	L 2
2142	M 2
2143	K 2
2144	K 3
2145	K 3
2146	O 4
2147	O 6
2148	O 7
2149	N11
2150	N11
2151	N11
2152	J 7
2153	K 7
2154	N 3
2155	O 3
2156	K 5
2157	K 5
2158	O 7
2160	A18
2161	A17
2162	B16
3101	D 5
3108	D 6
3110	C 9
3111	E 9
3112	D 9
3113	E10
3114	A14
3115	A12
3116	D15
3117	D16
3118	D11
3119	E11
3122	B 8
3123	B 8
3130	H14
3131	H14
3133	J 6
3135	H 7
3136	I 5
3140	I 1
3141	L 2
3143	O 6
3144	O 7
3145	N11
3146	J 6
3150	A17
3151	A17
5105	A12
5110	J10
5111	J11
5120	J 1
5121	J 1
5122	K 2
5123	K 2
5124	K 4
5125	O 5
5127	O 3
6104	C 2
6105	D12
6106	I 13
6110	J 7
6111	L10

Fig.3.1

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If AM signal are processed the procedure is different. It is good to know that the TEA6100 is suited for the processing of FM-IF and AM-IF signals but in the Cluster family the TEA6100 is only used in the AM mode for IF level data. There is a problem attached to it, however. The IF level detectors see the AM modulation as an IF level change and this is amplified by the level amplifier. On the DC voltage of pin 3 a detected and an amplified AF signal is superposed. This AF signal disturbs the required IF level data. We should thus in fact decouple the output of the level amplifier by means of an el.cap. for these AF signals, but then we would also decouple the multi-path data during FM reception, which is not desired. We will now first allow the signal to be amplified by the multi-path amplifier and not until then is the AF signal decoupled by means of el.cap. 2113 at pin 5. This el.cap. does no longer affect the multi-path data and at the same time the correct AM-IF level data is obtained. This data is also available at the I^2C bus via analogue/digital converter ADC-2.

- IF muting.

The IF soft-mute stage between the IF amplifier and the quadrature demodulator has been executed as an IF signal control. The advantage being that a gradual level control is possible. The soft-mute is driven by a DC voltage. The muting does not start functioning until the DC voltage at pin 3 goes below 1,5 V. If the voltage at pin 3 has dropped to 0 V, the IF level has been readjusted to a minimum. To prevent the soft-mute from introducing a kind of "on" / "off" effect as a result of rapid fluctuations in the aerial signal, it has been made possible to connect an external mute delay capacitor. See Fig. 3.1. Here the mute-delay capacitor consists of a parallel circuit of capacitor 2103 and el.cap. 2115. In principle the mute delay time is realized by a diode, a current source and the external capacity. The effect is that the muting is energized quickly while the signal slowly picks up again.
The combination of this soft-mute and the mute delay ensures that a ratio-detector-like behaviour is realized. So far this is the most desired situation as far as carradios are concerned.

Apart from the IF level the soft-mute can also be controlled by means of the afore-mentioned level control at pin 14. This control sees to the α-3dB point, but it is also possible to compensate for a spread in the front-end amplification. The maximum control range is approx 10 dB.

- Internal power provision

A voltage stabilizer (see Fig. 3.2) sees to the required line voltages. One of these line voltages is V_{ref} which is externally available at pin 15. It is possible to switch this voltage via the I^2C bus. This works in parallel with the AM/FM mode of the IC. The following voltages are available:

- FM mode: pin 15 = 4,3 V
- AM mode: pin 15 = floating

Internally this voltage is used to mute the AF output (pin 11) in the AM mode of the IC. Externally this voltage is applied for two matters.
In the first case V_{ref} is used as a stable voltage for IF level adjustment (α-3dB) at pin 14. See Fig. 3.1.
In the second case the switching function of 4,3 V in FM to "floating" in AM is used for external AM level adjustment. It is used for the search level adjustment. This adjustment also takes place at pin 14. Fig. 3.1 shows what the circuit looks like in practice.

In the FM mode of the IC the voltage at pin 14 only depends on the 4,3 V at pin 15 and the adjustment of trimming potentiometer 3113. If switching over to AM takes place now, the voltage at pin 14 will be determined by the +3a voltage and the resistor network 3110, 3111, 3112 and 3113.
The desired level is adjusted with trimming potentiometer 3111. The circuit used here implies that the AM/FM level adjustment is a semi-separate adjustment. This implies that first the FM-IF level and then the AM-IF level has to be adjusted because these two adjustments are interdependent.

3.2.4.2. Digital tuning interface section

Fig. 3.3 shows the block diagram of the digital tuning interface section. In principle 3 sections can be distinguished:

- AM/FM-IF counter
- An analogue/digital converter with two inputs for IF level and multi-path level.
- An I^2C bus interface.

- Set-up and working of the frequency counter

The IF counter is based on the time window principle and consists, apart from the programmable timebase, of an eight-stage frequency counter (dividend 2^8), a programmable prescaler, a time window circuit and a one-stage divider (dividend 2). The frequency is measured by counting the number of pulses within a certain period (time window). Of this periodic span of time we will assume T seconds as duration. Because the TEA6100 has to measure both AM-IF and FM-IF signals, T has been made adjustable by means of the I^2C bus. In case T is a large period, the resolution of the counter will increase, which will be necessary for measuring the FM-IF. The disadvantage of a high T is that the measuring speed decreases. To increase the freedom in the use of this IC a selection can be made between the measuring speed and the measuring accuracy. To realize this the divider by 2 between the frequency counter and the time-window has been made so that it can be switched off. If this divider is switched off, the system accuracy is approx 1 bit per measuring cycle. This corresponds with a deviation of 250 Hz for the AM-IF (IF = 460 kHz) and 6,4 kHz for the FM-IF (IF = 10,7 MHz). Now the measuring time is 4ms for AM and 20ms for FM. If an AM system with an IF of 10,7 MHz is applied, a much more accurate measurement is required than for an FM system with an IF of 10,7 MHz because the percentual counter deviation would be too great relative to the carrier frequency. This would make proper tuning impossible. That is why the deviation of the counter for an AM-IF of 10,7 MHz is only 500 Hz. Naturally the measuring time becomes much greater now. If the divider by 2 is switched on, the accuracy is 1/2 bit per measuring cycle. The deviation in the measured frequency is halved now, while the measuring time is doubled.
The measured values for the 8-stage frequency divider are via an 8-bit output gate applied to the I^2C bus, so that the FM data is available for the microcomputer. Then the microcomputer knows if the tuning is correct and may command the synthesizer to correct the tuning, if necessary.

- Processing of analogue signals on the I^2C bus.

The digitization of analogue data of the signal processing section takes place in the tuning interface section. The AM/FM intermediate frequency level and the multi-path level are via a TTL selector presented to a 3-bit analogue-digital converter. The output of the converter is via a multiplexer and a 2x3 bit output gate applied to the I^2C bus. In case of FM reception it is necessary that the TTL switch works in parallel with the multiplexer. The two inputs of the switch, namely the IF level and the multi-path level should both be available to the microcomputer.
Now the analogue switch will function as a multiplexer. The parallel IF level and multi-path data is presented serially to the A/D converter and then the digital signal is demultiplexed.
The digitized IF level and multi-path signal are both presented separately to a 3-bit output gate and applied to the I^2C bus. Via this system both data are available to the microcomputer. During AM reception multiplexing takes place as well, but now the microcomputer ignores the possible data which enters via the FM level measurements.

- Timing of the digital section

For control of the digital section a external clock signal is used. High demands are made on the stability of this clock, because the accuracy of the frequency counter directly depends on the accuracy of the clock. The counter uses this frequency as reference frequency. The system is suited for frequencies of 32 kHz or 40 kHz. In the Cluster family 40 kHz is applied, obtained from the SYMO-N (TSA6057). It has an internal crystal-controlled clock having a frequency of 4 MHz. This frequency is divided by 100 in the TSA6057 and presented to pin 9. The resultant 40 kHz has a high accuracy.

3.2.5 Data formats I^2C bus.

Communication between the TEA6100 and the microcomputer takes place via the well-known I^2C bus. Now attention will be paid to the data formats of the TEA6100.

- Write mode.

When the TEA6100 receives its address code (1100001) followed by a write bit (0) and a data byte, the IC is initialized and the frequency counter reset. The input data format is shown in Fig. 3.4. Now we will deal with the set-up of the input data byte.

Bit 1 Adapts timebase divider N1 to the presented reference frequency.
1 = 40 kHz
0 = 32 kHz

Bit 2 Selects the AM or FM mode of the analogue signal processing section.
1 = FM
0 = AM

Bit 3 Selects the AM or FM input, pin 18 or pin 19.
1 = pin 18
0 = pin 19

Bit 4 Adapts the prescaler for division of the IF signals of 460 kHz or 10,7 MHz.
1 = 10,7 MHz
0 = 460 kHz

Bit 5 Resets divider N1 and adapts the frequency counter for the AM mode or the FM mode.
1 = FM
0 = AM

Bit 6 Programmes the dividend of divider N1 and in this way a high or a normal accuracy of the IF counter is obtained (extension of the time window).
1 = division by 1
0 = division by 8

Bit 7 Switches the divider by two between the time window and the frequency counter on and off.
1 = on : accuracy ± 1/2 bit.
0 = off: accuracy ± 1 bit.

Bit 8 Switches the test mode on and off. In the test mode the reset signal of the frequency counter is internally connected to pin 5.
1 = test mode on.
0 = test mode off.

- Read mode.

When the IC receives its address code followed by a read bit (1) it is set to the read mode.
The results of the measurement are sent to the microcomputer.
This data is transmitted as two 8-bit words. The first byte contains data on the FM-IF level and the multi-path level. The second byte contains the IF code. The output data format is shown in Fig. 3.5.
If it is necessary the data transmission can be interrupted by ignoring the acknowledge bit which succeeds the first byte.

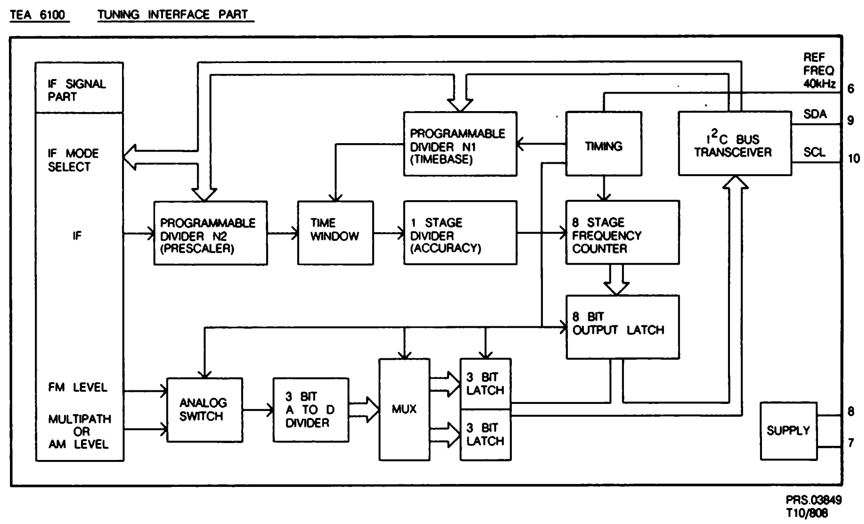

Fig.3.3

INPUT DATA

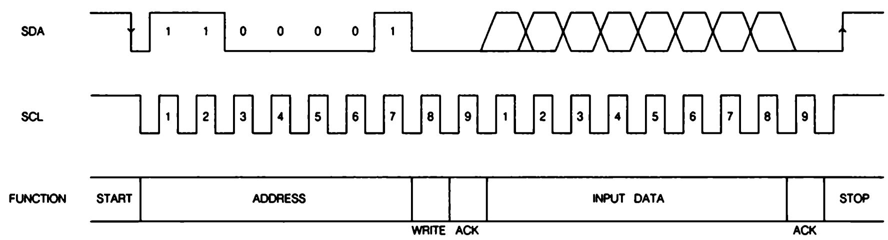

Fig.3.4

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T10/811

OUTPUT DATA

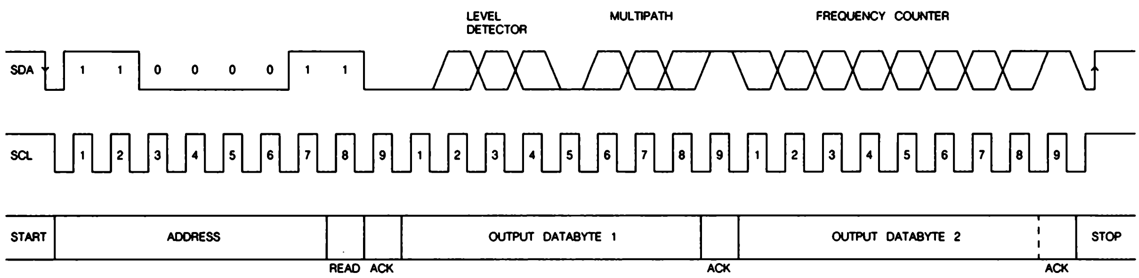

Fig.3.5

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T10/811

Chapter 4. AM section (RF + IF)

4.1. General.

The AM reception section in the Cluster family is based on IC TEA6200 (6111). In this IC both the RF section and the IF section are integrated. The striking thing of the IC is that it works at an IF of 10,7 MHz. The advantage is that with this system the oscillator frequency and the image frequency of the mixer are lying outside the waverange to be received. In illustration we take a reception frequency (Fw) of 600 kHz (MW). The assumption is that the AM–IF is 468 kHz.
Oscillator frequency (Fo) is calculated as follows:
Fo = Fw + IF [kHz]
Fo = 600 + 468 = 1068 kHz. This frequency is also lying in the MW band.
The image frequency of the mixer (Fs) is calculated as follows:
Fs = Fw + 2xIF [kHz]
Again the assumption is an Fw of 600 kHz.
Fs = 600 + 2x468 = 1536 kHz. This frequency too is lying in the MW range and will thus require strong suppression.
To circumvent these problems an AM–IF of 10,7 MHz has been selected. The first advantage is obvious now. The second advantage is that the filters are available for this frequency. Processing of 10,7 MHz AM–IF is all the more simpler since it can partially be done in the same way as the processing of 10,7 MHz FM–IF. Think for instance of the IF measuring system of the MUSTY–Q.

4.2. Function description of the TEA6200.

The circuit diagram of the AM section is shown in Fig. 3.1. To obtain a good insight into the working of the TEA6200 we have subdivided this IC in a number of functional blocks which will be discussed separately. Below follows a survey of the subdivision:

- Preamplifier.
- Bandpass filter.
- Mixer & VCO.
- IF selectivity.
- IF amplifier.
- Level output.
- Detector.
- Reference voltage.
- Stand–by function.

4.2.1. Preamplifier.

The preamplifier serves for the adaptation between the capactive aerial and the bandpass filter. Because the IC has to be capable of processing RF signals from the LW, MW and SW band, a wideband amplifier is required. Capacitor 2142 is a capacitive feedback which sees to the wideband character of the preamplifier but also for the required linearity and noise suppression. Pin 19 is the virtual ground.
The amplification of LW and MW signals is determined by the aerial capacity and 2141. If the aerial capacity is 15 pF and 2140 is 10 pF, the amplification will be 3 dB. In case of reception of SW (49m) signals the amplification will be 6 dB higher.
The cause is the series resonance of the two 10 µH coils 5120, 5121 and a total capacity of 90 pF.In its turn this 90 pF is a parallel circuit of the 15 pF aerial capacity, the cable capacity and the input capacity of the FM tuner module.
Resistor 3140 determines the quality factor (Q–factor) of the series resonance circuit. As a result of the 3dB higher amplification of SW signals the reception quality of this waverange will be slightly better compared with the LW and MW signals.

The second part of the circuit, consisting of 5120,5121 and 3140, determines the high–frequency behaviour. The circuit suppresses resonance frequencies of the aerial cable. These resonances develop because the capacity of the aerial cable also forms part of the feedback.

The amplification peak of the preamplifier is lying around 6 MHz. For high frequencies the amplification thus decreases, the advantage being that possible image frequencies are suppressed. This is especially important with strong transmitters because then the output of the preamplifier may introduce interference when the frequency difference is lying in the LW, MW or SW range. The amplification of the preamplifier is independent of the extent of the aerial signal. An exception is made when a very strong aerial signal in the order of 1V/m is presented. Then the preamplifier switches to a lower amplification factor. This has been done to prevent the preamplifier from clipping. To achieve switching–over a level detector has been connected to the output of the preamplifier. The output of this detector is connected to pin 1 so that that this one is also externally available. If the output level of the preamplifier exceeds a certain value, an additional capacitor 2142 is switched in parallel with the already existing feedback capacitor 2141 and this additional capacitor reduces the overall amplification by 12 dB. Then the amplification is –9 dB. If the output level of the preamplifier drops by in total 16 dB, the amplification switches back to normal level.

4.2.2. Bandpass filter

The purpose of the bandpass filter is the suppression of the image frequency of the mixer which is fed back to the output of the preamplifier. The filter should, however, allow the frequencies to be received to pass. As we have seen in chapter 4.1. the image frequency is calculated as follows:

Fs = Fw + 2xIF [Hz]

If this is applied on the LW and MW band (150 kHz – 1,6 MHz) this Fs is lying between 21,55 MHz and 23,0 MHz. The filter used is an asymmetric Chebyshev filter consisting of components 3141, 5122, 2143, 5123, 2144 and 2145 (see Fig. 3.1). The frequency range that is allowed to pass is suppressed by 1 dB. The –3 dB points are lying at 100 kHz and 1,8 MHz with the values used in Fig. 3.1. The low –3 dB point is determined by decoupling coil 5124 and by filter input resistor 3141. Coil 5124 is also needed for the DC voltage adjustment of the mixer. With the filter dimensioning as indicated in Fig. 3.1. the image frequencies are suppressed by 70 dB. If a capacity of 1 pF is present between the input of the mixer (pin 2) and the preamplifier output (pin 20), the suppression of the image frequency becomes worse than 50 dB. It is thus important to prevent a stray capacity. If the carradio is also suited for reception of the SW band the bandpass filter will have to be adapted. The frequency band to be allowed to pass will then range from 150 kHz to 6,2 MHz.

4.2.3. Mixer & VCO.

4.2.3.1. Mixer.

The mixer applied is double–balanced mixer. The amplification of the mixer for 10,7 MHz is –1 dB while the frequencies beyond it are amplified by +5 dB. This amplification has been defined as the voltage amplification at a load impedance of 1 kΩ. The impedance for 10,7 MHz is considerably lower, namely 500 Ω.

4.2.3.2. VCO.

The VCO has been equipped with a parallel resonance circuit. This circuit consists of components 5126,2152 and varicap 6110. By means of 3146,2130 and 3133 the DC voltage control for the VCO is decoupled for the oscillator signal. The output level of the oscillator is controlled internally, although the amplification of the mixer is independent of the oscillator level. The sidebands of the VCO, however, do depend on the oscillator level. The Q–factor of the resonance circuit should be as high as possible for maximum suppression of the sidebands.

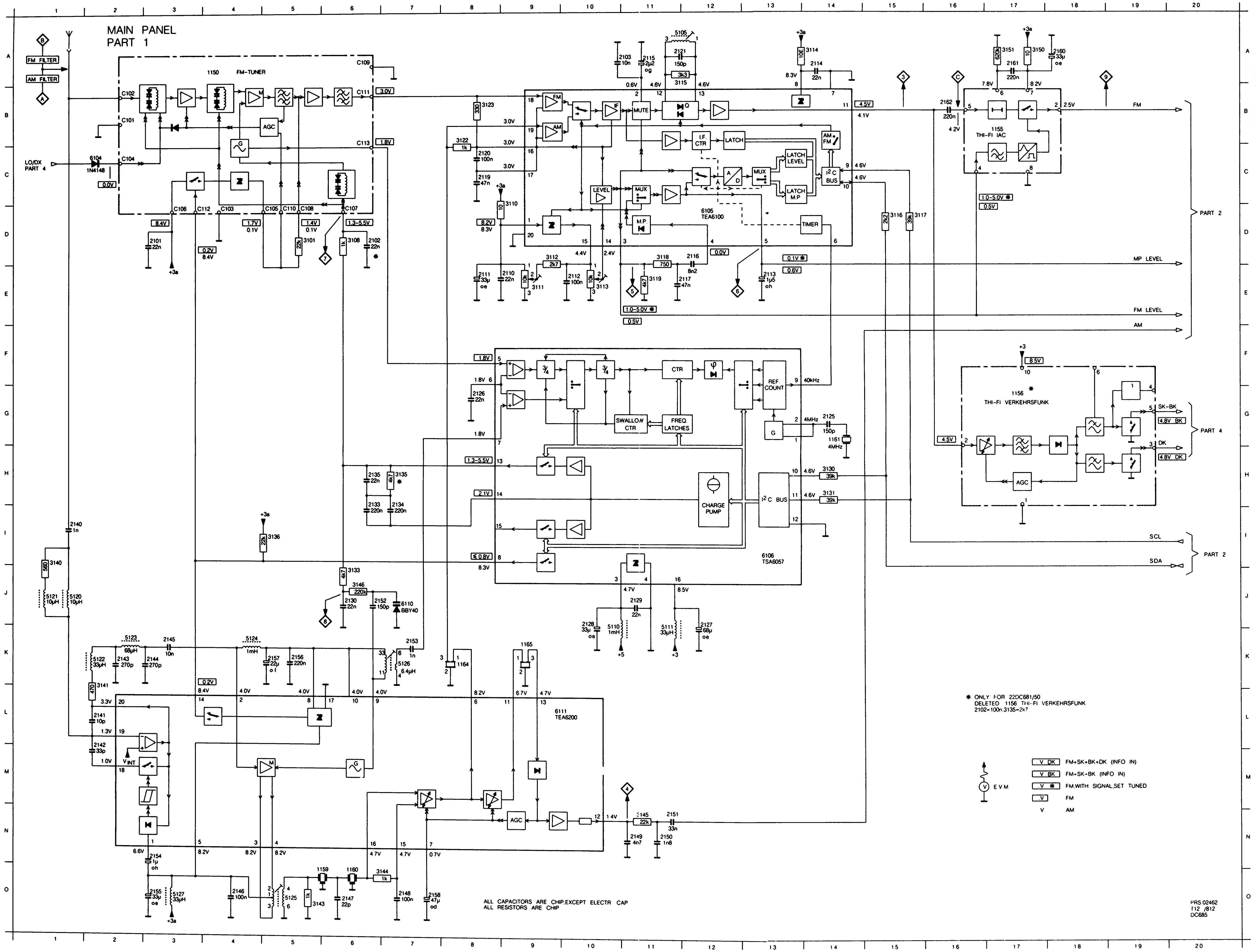


Fig.3.1

1150	A 4
1155	B17
1156	G17
1159	O 6
1160	O 6
1161	G14
1164	K 8
1165	K 9
2101	D 3
2102	D 6
2103	A11
2110	E 9
2111	E 8
2112	E10
2113	E13
2114	A14
2115	A11
2116	D12
2117	E12
2119	C 8
2120	C 8
2121	A11
2125	G14
2126	G 8
2127	J12
2128	J10
2129	J11
2130	J 6
2133	H 6
2134	H 7
2135	H 6
2140	I 1
2141	L 2
2142	M 2
2143	K 2
2144	K 3
2145	K 3
2146	O 4
2147	O 6
2148	O 7
2149	N11
2150	N11
2151	N11
2152	J 7
2153	K 7
2154	N 3
2155	O 3
2156	K 5
2157	K 5
2158	O 7
2160	A18
2161	A17
2162	B16
3101	D 5
3108	D 6
3110	C 9
3111	E 9
3112	D 9
3113	E10
3114	A14
3115	A12
3116	D15
3117	D16
3118	D11
3119	E11
3122	B 8
3123	B 8
3130	H14
3131	H14
3133	J 6
3135	H 7
3136	I 5
3140	I 1
3141	L 2
3143	O 6
3144	O 7
3145	N11
3146	J 6
3150	A17
3151	A17
5105	A12
5110	J10
5111	J11
5120	J 1
5121	J 1
5122	K 2
5123	K 2
5124	K 4
5125	O 5
5127	O 3
6104	C 2
6105	D12
6106	I 13
6110	J 7
6111	L10

The optimal value for coil 5126 to realize this is 6,4 µH. The concept of the oscillator is such that the coil need not be adjusted (core in nominal position).
With varicap diode 6110 (BBY40) and coupling capacitor 2152 (150pF) the VCO can be tuned between 10,85 MHz and 12,35 MHz. The corresponding tuning voltage will then lie between 1V and 6,5V.

4.2.4. Intermediate frequency selectivity

The balance output of the mixer is converted into an asymmetric output by means of output transformer 5125. To this coil also applies that it need not be adjusted. Since the output of 5125 is rather heavily loaded with 1 kΩ (3143) this circuit will be damped strongly, causing the Q–factor to decrease. In this way a large bandwidth is accomplished. Next follows filtering of the IF signal. This filtering deserves some attention. Contrary to FM reception with an IF of 10,7 MHz , AM reception with an IF of 10,7 MHz requires a much higher selectivity. The cause is that the frequency difference between the underlying AM transmitters is only a fraction of the the 10,7 MHz IF. With an aerial voltage of 700 µV the selectivity of the system applied here is 10 kHz. This 10 kHz is about 0,93 promille of 10,7 MHz; this makes it necessary to filter very accurately. To obtain a sharp filter characteristic two crystal filters (1159, 1160) are applied. The filter properties of a ceramic filter are not sufficient for this application. The total filter, consisting of 3145, 1159, 2147, 1160 and 3144 only determines the selectivity and that is why it is very important not to have capacitive feedback between pins 3,4 and pin 16 of the IC. This would be very detrimental to the selectivity. To prevent this feedback a ground conductor has been applied in the copper pattern on the PCB of the carradio. This is the minimum requirement.

4.2.5. IF amplifier

The IF amplifier, consisting of two stages, amplifies the filtered IF signal to the correct level for the demodulator. The amplifier has a differential input, pins 15 and 16, of which pin 15 is coupled to ground via 2148 for AC voltage. Internally this pin 15 is also used for the DC voltage adjustment of the amplifier.
The output of the IF amplifier (pin 11) is via a ceramic filter fed to the detector input (pin 13). This filter has two functions. On the one hand it serves for noise suppression and on the other hand for suppression of interference.

Noise suppression is necessary because the IF amplifier has a large bandwidth and thus adds noise to the IF signal. Since the AM detector is not selective the related noise would be added to the demodulated AF signal.
The interference is the result of a capacitive coupling between the relatively high–ohmic input of the IF amplifier (pin 16) and the VCO output (pin 9).

For aerial signals of 50µV or more the IF amplifier gives a constant output signal. El.cap. 2158, which is connected to pin 7, determines the bandwidth of the AGC circuit. By this bandwidth we mean the reaction speed at which the AGC interferes. Unfortunately, this el.cap. cannot simply be increased or decreased. Increase result in less distortion for low modulation frequencies but at the same time causes a delay of the AGC working. A decrease thus accelerate the reaction speed of the AGC but the distortion for the low modulation frequencies also increases. The value of this el.cap. should thus be determined empirically.

4.2.6. Level output.

Pin 6 is the level output of the TEA6200. This signal makes it possible to determine the IF level and thus to determine if the transmitter tuning is correct. At aerial voltages ⩽ 10mV the level varies. At a higher level the IF level remains constant.

The signal of pin 6 can be connected directly to the IF input of the MUSTI–Q, but some problems present themselves, which have also been discussed in section 4.2.5. The wide–band IF amplifier adds noise to the level output and here too interference with the VCO signal occurs. This has also been solved by sending the signal from pin 6 through a ceramic filter (1164). The requirements posed on the filter are that it should have a limited bandwidth and that it should properly suppress the VCO frequency. The minimum VCO frequency is obtained during tuning to the lowest LW station in the band, 150 kHz. The VCO frequency will then be 10,85 MHz. A ceramic filter suppresses this frequency to a sufficient degree.

4.2.7. Detector

From ceramic filter 1165 the IF signal appears at the detector input, pin 13. The input voltage is 5 mV. This voltage is kept as constant as possible by the IF amplifier in combination with the AGC circuit. The input impedance of the detector relative to ground is 330 Ω. At an input voltage of 5 mV the detected AF output level is 350 mV with open output. The output impedance is 10 kΩ. The detected signal, which appears at pin 12, is presented to a lowpass filter. This lowpass filter consists of components 2140, 3145 and 2150. With the dimensioning of the filter, as shown in Fig. 3.1, the bandwidth is 2 kHz. Naturally, the bandwidth can be increased in order to realize a better audio spectrum. The disadvantage is that the noise level would also be increased.
The filter in the Cluster family has been dimensioned so that for the human ear the best signal–to–noise ratio is obtained.

4.2.8. Reference voltage

For internal DC voltage adjustments the TEA6200 has been equipped with a reference voltage of 4V. This voltage is also available externally at pin 8 for possible other purposes. If this voltage is used, it has to be decoupled carefully because otherwise the S/N ratio of the IC will drop considerably.

4.2.9. Stand–by function

Pin 14 is the stand–by connection of the IC. If this pin 14 is logically "1" the IC starts to work, while logical "0" is the stand–by mode. The power consumption will drop to 20% of the orginal value then.
In the stand–by mode of the IC not a single function is operational.

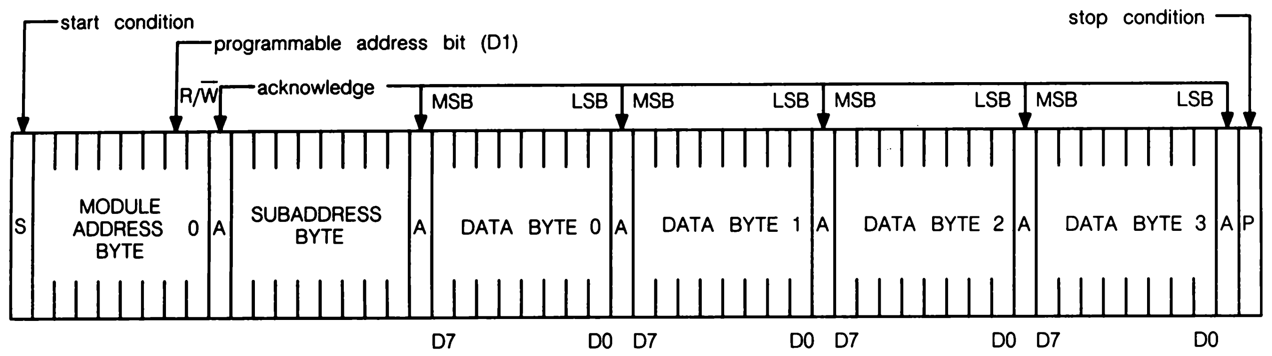
Chapter 5. Transmitter tuning

The Cluster family has been provided with a PLL tuning system. The applied synthesizer is the TSA6057 (6106) (See Fig. 3.1).
The TSA6057 communication via the I²C bus with the microcomputer. In the next section this IC will be studied in more detail.

5.1. Function description of the TSA6057.

Via outputs pins 7 and 5 the AM VCO and the FM VCO signals respectively can be presented. The AM VCO frequency is allowed to lie between 0,512 MHz and 30 MHz. For the FM VCO frequency the values are 30 MHz and 150 MHz. The VCO signal is first divided in a prescaler. For AM the dividend is 3 or 4, while for FM the dividends are 15 or 16. By means of the I²C bus the AM or the FM signal can be selected via the multiplexer. The related VCO signal is divided by a programmable 13–bit counter and presented to a digital phase detector with memory.

BIT ORGANIZATION TSA6057



	MSB							LSB
MODULE ADDRESS	1	1	0	0	0	1	0/1	1
	D7							D0
SUBADDRESS	0	0	0	0	0	0	0/1	0/1
DATA BYTE 0 (DB0)	S6	S5	S4	S3	S2	S1	S0	CP
DATA BYTE 1 (DB1)	S14	S13	S12	S11	S10	S9	S8	S7
DATA BYTE 2 (DB2)	REF1	REF2	FM/$\overline{AM}$	$\overline{FM}$/AM OPAMP	NOT USED	BS	S16	S15
DATA BYTE 3 (DB3)	T1	T2	T3	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED

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Fig.5.1

There the divided VCO signal is compared with a very stable reference frequency, which is obtained through division of the internal clock signal. The frequency of it is 4 MHz. The divider produces four different frequencies: 40 kHz, 25 kHz, 10 kHz and 1 kHz. The 40 kHz signal is, as has become clear in the meantime, intended as reference frequency for the MUSTI–Q. The other three frequencies are intended as reference frequencies for the phase detector. The TSA6057 has also been provided with a programmable current source (charge pump). This pump may deliver two different currents, viz 5μA and 450μA. The greater current is used when it is necessary to tune to a transmitter and this has not yet been realized. 5μA is used for stable tuning. For switch–over from AM to FM and vice versa, use can be made of an internal switch, which is connected to pin 8. Via the I²C bus this pin can be switched to ground or made floating. Now we will discuss the digital control section in more detail.

5.2. Data formats of the TSA6057

To program the IC a start condition has to be given, followed by a module address byte and a write bit (0). Next follow an acknowledge bit, a sub–address byte, an acknowledge bit and four data bytes (see Fig. 5.1). The sub–address determines which of the four data bytes is transmitted first.
The module address contains a programmable address bit (D1) and together with the address input (pin 12) this bit makes it possible to work with two synthesizers in one system. In the Cluster family this does not apply.
The auto–increment feature of the I²C bus makes it possible to program the TSA 6057 with one single data transmission. If desired, the IC can also be programmed partially. Then each transmission should end with a stop condition.

The bit organization is shown in Fig. 5.1. It shows the set–up of a complete data transmission. It consists of six bytes preceded by a start condition and terminated by a stop condition. Each byte is followed by an acknowledge bit. Furthermore, the bytes have been interleaved so that it becomes clear which information is present in which bit and/or byte.
Data byte 3 can be used for test purposes and should in this case be filled with zeroes.
To clarify the meaning of the bits they will be studied in more detail.

Bits S0 through S16 (data bytes 0, 1 and 2) are together with bit FM/$\overline{AM}$ used to determine the dividend of the frequency (f_i) at inputs AM_1 (pin 7) and FM_1 (pin 5).
Fig. 5.2 shows the set–up of the dividend.
F_{ref} is the reference frequency which is presented to the phase detector.

FM/$\overline{AM}$	Input frequency (f_i)	Input
0	$(S0x2^0 + S1x2^1 + S13x2^{13} + S14x2^{14}) \times f_{ref}$	AM_1
1	$(S0x2^0 + S1x2^1 + S15x2^{15} + S16x2^{16}) \times f_{ref}$	FM_1

Fig. 5.2

The minimum dividend in the AM mode is: $2^6 = 64$
The minimum dividend in the FM mode is: $2^8 = 256$

The CP bit (Charge Pump), which is bit 0 of data byte 0, is used for control of the charge pump. Fig. 5.3 shows the effect of this bit.

CP	current
0	low
1	high

Fig. 5.3

In practice "current low" comes down to a previously mentioned current of 5μA. With "current high" the current is 450μA.

By means of the REF1 and REF2 bits, which are present in data byte 2, the reference frequency is selected, which is used by the phase detector. Fig. 5.4 shows the truth table for this situation.

REF1	REF2	frequency kHz
0	0	1
0	1	10
1	0	25
1	1	none

Fig. 5.4

The FM/AM OPAMP bit controls the internal switches present at loop filter outputs pins 13 and 15. They are not used in the Cluster sets. The loop filter of the Cluster family can process both AM and FM tuning voltages and is connected to pin 13. For the sake of completeness Fig. 5.5 gives the settings of this bit.

$\overline{FM}$/AM OPAMP	pin 15 switch FM/AM	pin 13 switch AM/FM
1	closed	open
0	open	closed

Fig. 5.5

The last to which we will pay attention is bit 3 of data byte 2, the BS (BandSwitch) bit. As explained earlier this bandswitch can be used for switch–over of the waverange. Fig. 3.1 shows that pin 8 is connected to the stand–by connections of the FM tuning module and the TEA6200, so that it can be selected via the I²C bus.
Fig. 5.6 shows the effect of this bit.

BS	bandswitch output
1	sink current
0	floating

Fig. 5.6

"Sink current" refers to the current through the closed collector circuit of a transistor. In this case the voltage at pin 8 will no longer be 0,8 V. "Floating" refers to a floating or open output. The voltage is not allowed to be more than 12 V.

Chapter 6. Stereo/Dolby PCB

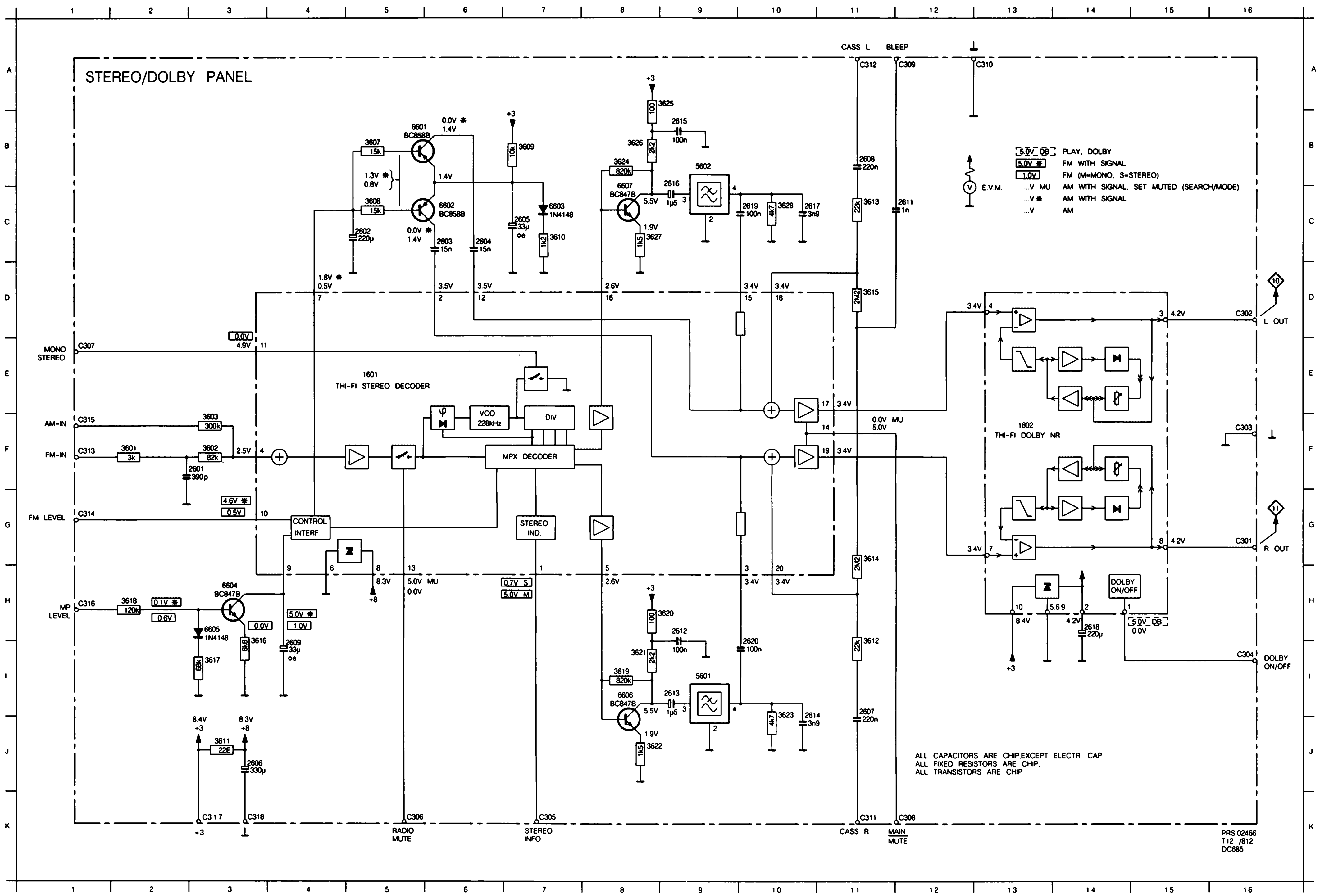
6.1. General.

If we re–examine the block diagram in Fig. 2.1, we see that the stereo/Dolby PCB occupies a central position. The microcomputer is responsible for most of the functions to be controlled. Only the FM–IF and multi–path level signals are coming from the MUSTY–Q and are used for the SDS and SDR control. The circuit diagram of the stereo/Dolby PCB is shown in Fig. 6.1. As mentioned before in chapter 2 the technique applied does not deviate much from what was applied before. The Dolby thick film has also been used in the PLL family. The stereo decoder thick film, however, does deserve some attention in the next section.

6.2. Description of the stereo decoder thick film

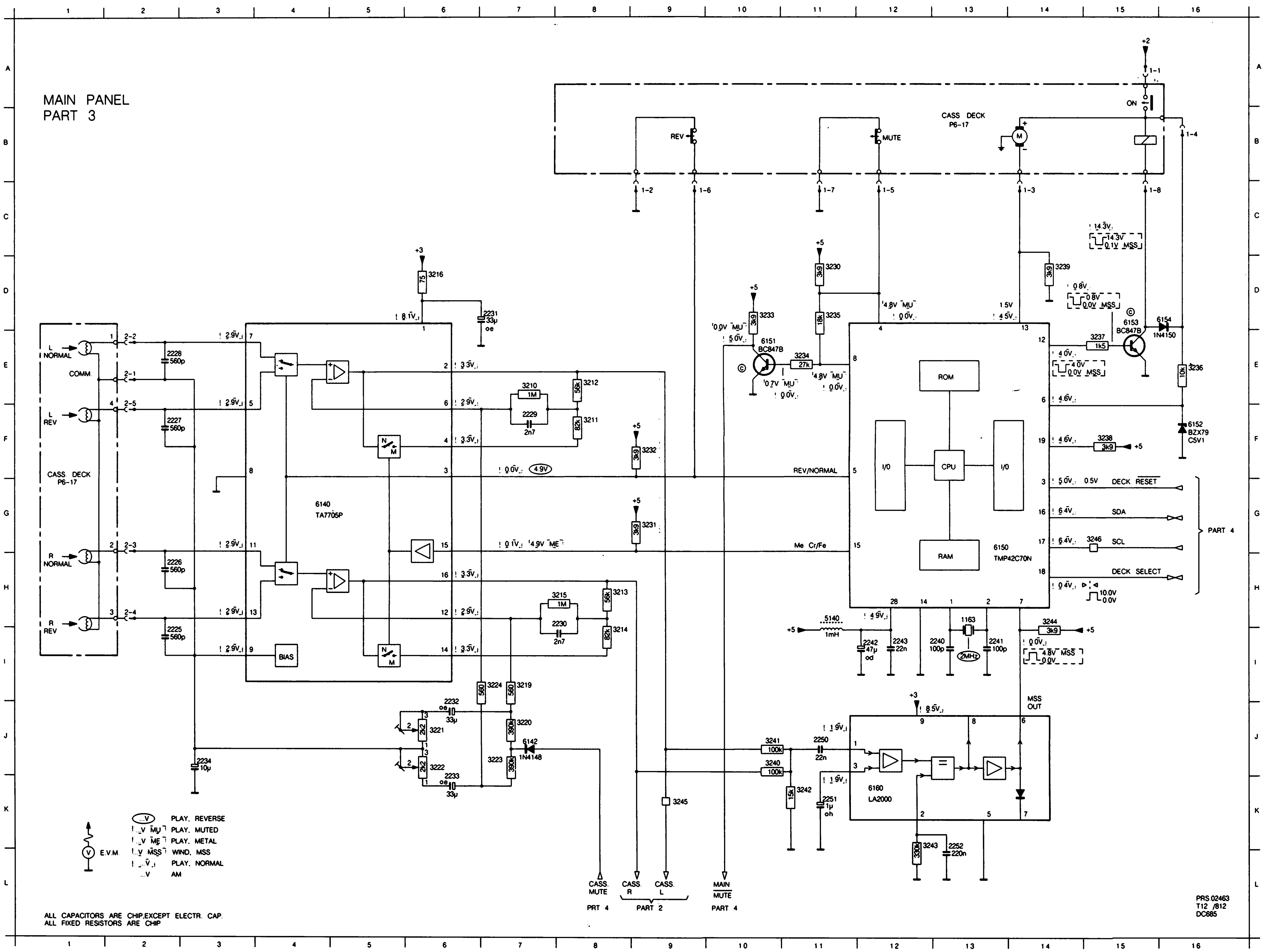
The TEA5581T is a flat–pack stereo decoder which is used on the thick film unit. It is the successor of the frequently used TEA5580, with a number of differences. The TEA5581T has been equipped with a source selector, a mute circuit and an output amplifier whose amplification can be set by means of an external resistor. This preset resistor is situated on the thick film so that the amplification is fixed. The outputs of these amplifiers are connected to pin 17 (left–hand channel) and pin 19 (right–hand channel) of the thick film. At the inputs of each amplifier an adder circuit is present. This circuit sees to adaptation of the two inputs present to the amplifier. One input is used for the AF signal of the cassette player and the bleep signal (pin 18 for the left–hand channel and pin 20 for the right–hand channel) while the other input is used for the AF–FM signal (pin 15 for the left–hand channel and pin 3 for the right–hand channel). Pins 2 and 12 of the thick film are used for connection of the SDR circuit. These aditional inputs serve to affect the input impedance of pins 3 and 15 as little as possible when the SDR control becomes effective. If the input impedance were to change, detuning of the pilot filters (5601 and 5602) might occur, resulting in a reduction of the suppression. Because the radio sound may not be audible during cassette playback, the IC has been equipped with a radio mute connection (pin 13 of the thick film). If the voltage at pin 13 is "high", the mute becomes effective and cassette playback can take place.
The TEA5581T also offers the possibility of muting the audio outputs (pins 17 and 19). The muting can be activated by rendering the main mute signal at pin 14 "low". This main mute signal is coming from the microcomputer (6150) for the cassette player control (see Fig. 6.2) or from the main microcomputer (6166) (see Fig. 8.1). This signal should be ≤ 0,8 V. If the muting is active the radio or cassette sound is suppressed by 90 dB. This takes place in the following cases:

- During ejection of the cassette.
- During manual or automatic searching.
- During fast forward or rewind.
- During switch–over from normal play to reverse play and vice versa.



1601	E 5
1602	F13
2601	F 3
2602	C 5
2603	C 6
2604	C 6
2605	C 7
2606	J 3
2607	I 11
2608	B11
2609	I 4
2611	C12
2612	H 9
2613	I 9
2614	I 10
2615	B 9
2616	B 9
2617	C10
2618	H14
2619	C10
2620	H10
3601	F 2
3602	F 3
3603	F 3
3607	B 5
3608	C 5
3609	B 7
3610	C 7
3611	J 3
3612	H11
3613	C11
3614	G11
3615	D11
3616	H 3
3617	I 3
3618	H 2
3619	I 8
3620	H 9
3621	I 8
3622	J 8
3623	I 10
3624	B 8
3625	A 9
3626	B 8
3627	C 8
3628	C10
5601	I 9
5602	B 9
6601	B 5
6602	B 5
6603	C 7
6604	H 3
6605	H 3
6606	I 8
6607	B 8

Fig.6.1



1163	H13
2225	I 2
2226	H 2
2227	F 2
2228	E 2
2229	F 7
2230	H 8
2231	D 7
2232	I 6
2233	K 6
2234	J 3
2240	I 13
2241	I 13
2242	I 12
2243	I 12
2250	J11
2251	K11
2252	K13
3210	E 7
3211	F 8
3212	E 8
3213	H 8
3214	I 8
3215	H 8
3216	D 6
3219	I 7
3220	J 7
3221	J 6
3222	J 6
3223	J 7
3224	I 7
3230	D11
3231	G 9
3232	F 9
3233	D10
3234	E11
3235	D11
3236	E16
3237	E15
3238	F14
3239	D14
3240	J10
3241	J10
3242	K11
3243	K13
3244	H14
3245	K 9
3246	G14
5140	H11
6140	G 4
6142	J 7
6150	G13
6151	E10
6152	F16
6153	D15
6154	D16
6160	K12

Fig.6.2

CS 16 734

Chapter 7. Low-frequency section

7.1. General.

The circuit diagram of the low-frequency section is shown in Fig. 7.1.
From the stereo/Dolby PCB the audio signal goes via capacitors 2177 (right-hand channel) and 2178 (left-hand channel) to the TEA6310T. This IC is the SOFAC (SOund FAder Control) which is responsible for all sound controls. The four sound signals which come from the SOFAC go via a DC voltage decoupling to the line out bus and also to the output amplifiers. Between the SOFAC and the output amplifiers another transistor circuit is present. In section 7.5 the purpose and the working of this circuit is described.
We will first discuss set-up and working of the SOFAC.

7.2. Introduction of the TEA6310T.

The SOFAC is a tone and volume control circuit for application in carradios. In the Cluster family the flat pack version of it has been applied. In the IC the following controls have been integrated:

- Volume and balance control. The control range is 86 dB in steps of 2 dB.
- Control of bass and treble. The control range of the treble goes from −12 dB to +12 dB in steps of 2 dB. The control range of the bass goes from −12 dB to +15 dB in steps of 2 dB.
- Fader control from 0 dB to −30 dB in steps of 2 dB.
- Low-noise signal processing so that the IC is suited for Dolby B and C noise suppression.
- Plop-free on/off circuit.
- Fast muting.
- I²C bus control of all functions.

In the next section we will discuss the working of these controls.

7.3. Function description of the TEA6310T

Signal control takes place via a series circuit of a number of resistors in combination with operational amplifiers which possess several inputs. By means of TTL switches and the related series resistors a step-variable resistance has been created. In this way signal control takes place. The advantage of this principle is a low distortion, a low noise level and a large dynamic range.

The IC is equipped with separate volume control for the left-hand and the right-hand channels. The advantage being that an additional balance control is not required.

The tone control section requires four additional components: 2170 and 2171 for the bass control while 2173 and 2174 serve for the treble control.

The TEA6310T has four AF outputs and is also provided with a fader control which is independent of the volume control. Via pin 9 of the IC this fader can be switched on and off. If the voltage at pin 9 is between 3V and 12V the fader is released. This is the case when four loudspeakes are connected to the carradio. The fader is switched off when the voltage at pin 9 is < 1,5 V, so that it is possible to make use of an AF output power of 2 x 20 W. In the four outputs of the TEA6310T four operational amplifiers are present which are connected with the I²C bus. These operational amplifiers have two functions. First of all via this way it possible to simultaneously mute the four AF outputs. This muting is activated via the GMU (General Mute) bit. This muting can be switched on and off via the Main Mute signal of the microcomputer (pin 5). This signal is logically "low" active. In chapter 6.2 you can find when activation is the case.

The second function of the operational amplifiers consists in bringing the AF outputs of the IC to such a level that they are suited for direct connection to the Line out bus. Furthermore, the operational amplifiers possess a low output impedance. For the TEA6310T the output impedance is lying around 100 Ω. The advantage of this low impedance is a low sensitivity for external interference sources.
To avoid switching on and off plops the TEA6310T has been provided with a plop suppression circuit. If the power supply voltage is switched on or off, a reset takes place, setting the IC temporarily to the general mute mode.

7.3.1. Signal control

All signal controls take place via the I²C bus. The data is coming from the microcomputer. On chapter 7.4 an explanation is given on the set-up of the commands.
To enable realization of all audio controls four selectors and a rotary switch have been incorporated in the matrix of the microcomputer (see Fig. 8.2). With each of the four selectors a sound control can be selected and then the related control can be affected with the rotary switch. The data which is in this way presented to the microcomputer is by this microcomputer converted in the I²C bus format of the TEA6310T. The microcomputer should thus contain a translation programme which has been laid down in the software. This translation programme should thus also contain the characteristic of a certain control. For volume control a logarithm control is desired while for tone control often a linear characteristic is applied. An advantage is that via the software application of the characteristic is possible. This is used in the loudness circuit. If the loudness key is pressed the microcomputer starts to adapt the normal translation programme for the tone control. This adaptation has also been laid down in the software, so that it is possible to lay down the loudsness characteristic. It is possible to make the loudness dependent on the volume, but also to affect the bass or the treble at option. In the Cluster family the bass and treble are affected while there also is dependence on the volume.

If the carradio is switched on, the TEA6310T is in the volume control mode. This control has the highest priority. If another control is selected the microcomputer switches back to the volume control after a while (± 10 s). Fast switch-back to volume control is possible when after selection of a sound control the related selector is pressed a second time.
If the carradio is switched off all modes of the sound controls are stored in the memory so that they are available again upon switching on, with the exception of the volume control. Upon switching on the volume is tied to a maximum. Low volume modes are remembered while higher volume modes are for the sake of safety overwritten by the maximum laid down in the software.

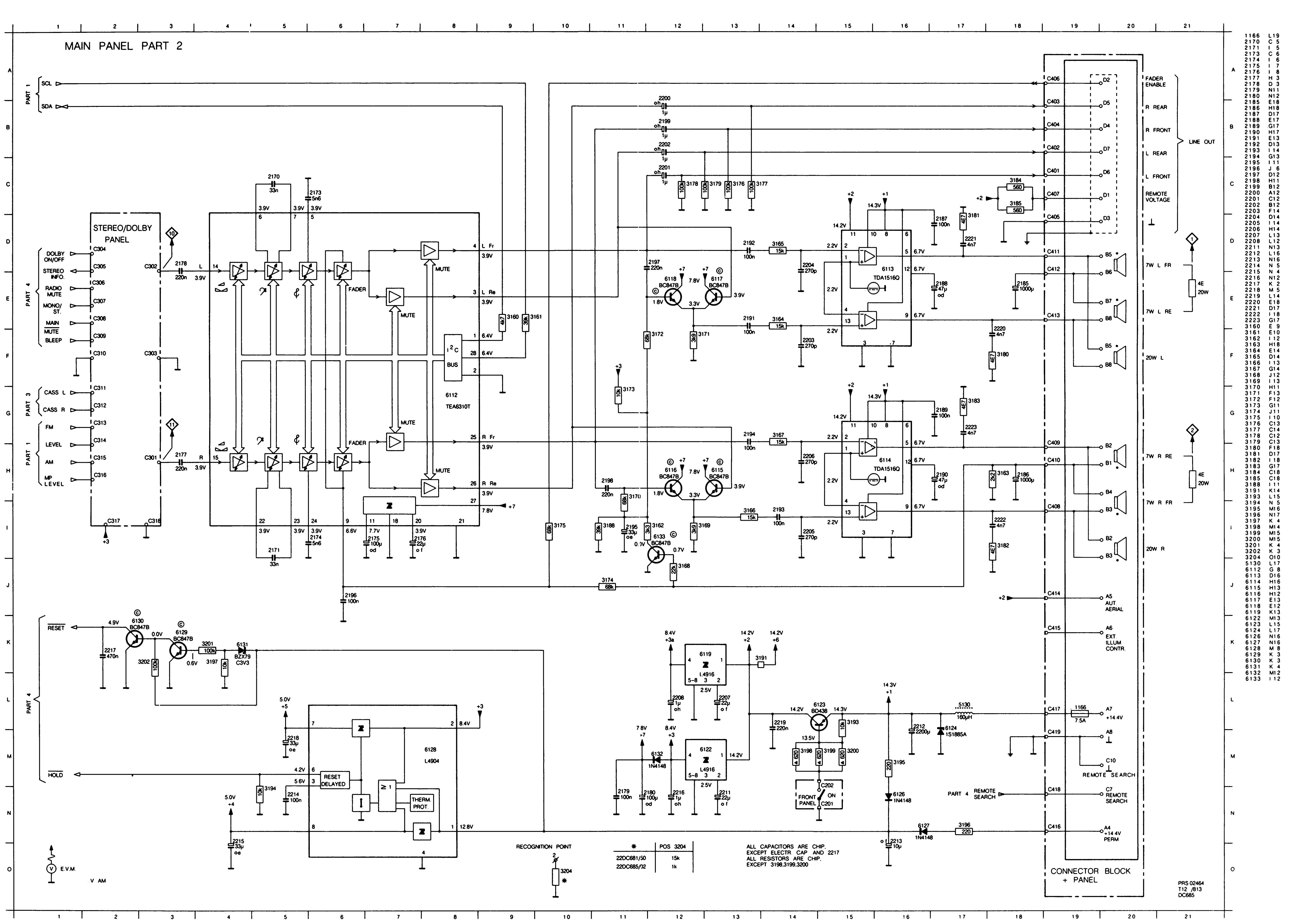


Fig.7.1

7.4. formats of the TEA6310T.

The set-up of the data transmission for the TEA6310T is shown in Fig. 7.2. To enable writing in the IC a start condition has to be given, followed by a module address (slave address). The SOFAC generates an acknowledge bit to signal the microcomputer that it is ready for further data reception. The microcomputer gives the sub-address to the SOFAC. This sub-address determines the control that will take place. If the sub-address has been received, the SOFAC responds with an acknowledge bit.

Now follows the data that is responsible for the mode of the addressed control. If the data has been received, the SOFAC again responds with an acknowledge bit and then the microcomputer terminates with a stop condition.

Below follows a survey of the functions of the data bits:

VL0 through VL5	Volume control left-hand channel.
VR0 through VR5	Volume control right-hand channel.
BA0 through BA3	Bass control.
TR0 through TR3	Treble control.
FA0 through FA3	Fader control.
FCH	Selection of fader channel (front or rear).
MFN	Makes it in combination with the FCH bit possible to mute one of the fader channels.
SCA through SCC	Control of the source selection (does not apply in the Cluster family).
GMU	Muting of the four AF outputs.

BIT ORGANIZATION TEA6310T

START CONDITION — ACKNOWLEDGE — STOP CONDITION

S	SLAVE ADDRESS	A	SUB ADDRESS	A	DATA	A	P

SLAVE ADDRESS = 1000000

FUNCTION	SUB-ADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
VOLUME LEFT	00000000	—	—	VL5	VL4	VL3	VL2	VL1	VL0
VOLUME RIGHT	00000001	—	—	VR5	VR4	VR3	VR2	VR1	VR0
BASS	00000010	—	—	—	—	BA3	BA2	BA1	BA0
TREBLE	00000011	—	—	—	—	TR3	TR2	TR1	TR0
FADER	00000100	—	—	MFN	FCH	FA3	FA2	FA1	FA0
SWITCH	00000101	GMU	—	—	—	—	SCC	SCB	SCA

— = DO NOT CARE

MDA.01332
T27/822

Fig. 7.2

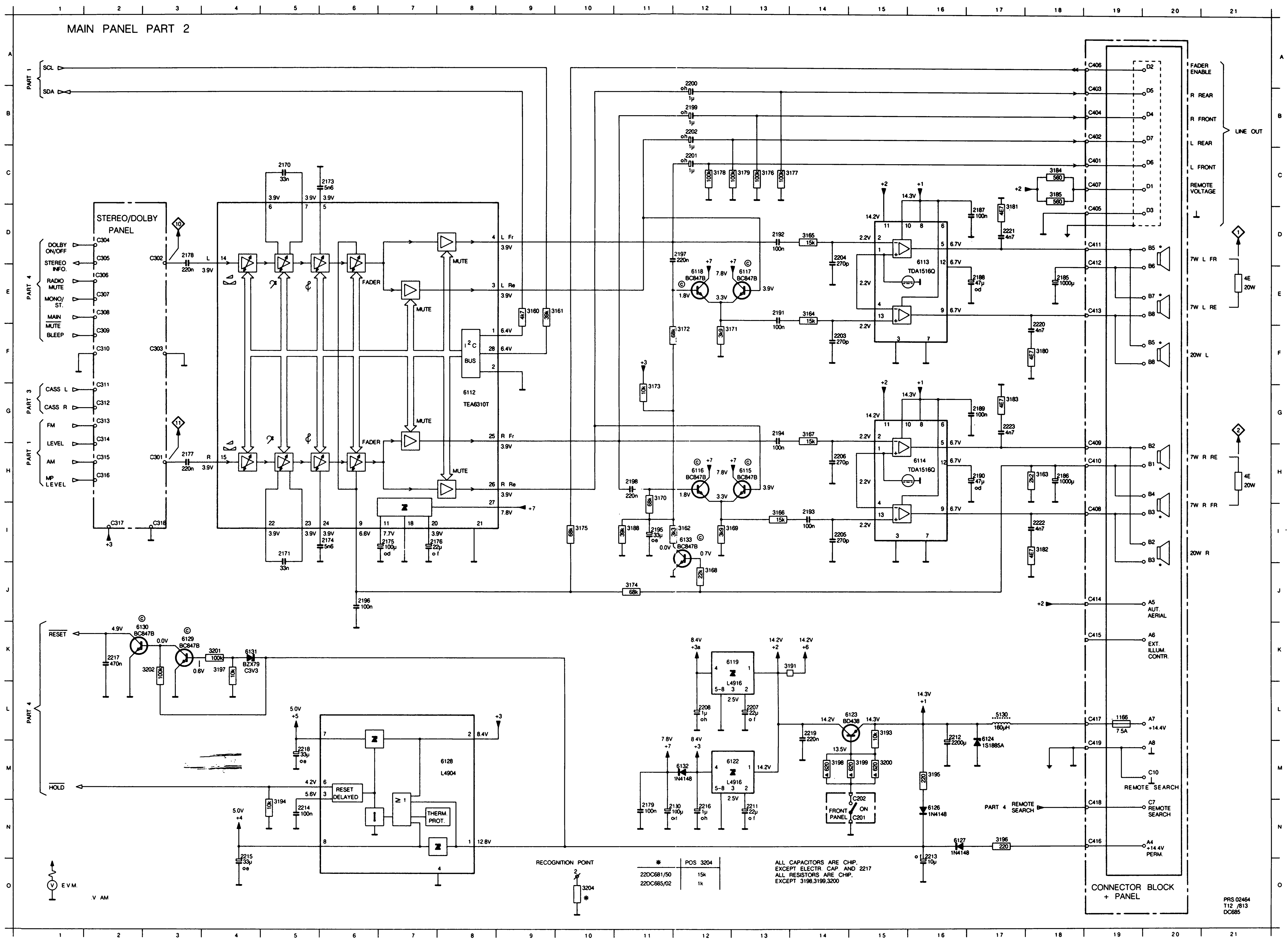


Fig.7.1

1166	L19
2170	C 5
2171	I 5
2173	C 6
2174	I 6
2175	I 7
2176	I 8
2177	H 3
2178	D 3
2179	N11
2180	N12
2185	E18
2186	H18
2187	D17
2188	E17
2189	G17
2190	H17
2191	E13
2192	D13
2193	I 14
2194	G13
2195	I 11
2196	J 6
2197	D12
2198	H11
2199	B12
2200	A12
2201	C12
2202	B12
2203	F14
2204	D14
2205	I 14
2206	H14
2207	L13
2208	L12
2211	N13
2212	L16
2213	N16
2214	N 5
2215	N 4
2216	N12
2217	K 2
2218	M 5
2219	L14
2220	E18
2221	D17
2222	I 18
2223	G17
3160	E 9
3161	E10
3162	I 12
3163	H18
3164	E14
3165	D14
3166	I 13
3167	G14
3168	J12
3169	I 13
3170	H11
3171	F13
3172	F12
3173	G11
3174	J11
3175	I 10
3176	C13
3177	C14
3178	C12
3179	C13
3180	F18
3181	D17
3182	I 18
3183	G17
3184	C18
3185	C18
3188	I 11
3191	K14
3193	L15
3194	N 5
3195	M16
3196	N17
3197	K 4
3198	M14
3199	M15
3200	M15
3201	K 4
3202	K 3
3204	O10
5130	L17
6112	G 8
6113	D16
6114	H16
6115	H13
6116	H12
6117	E13
6118	E12
6119	K13
6122	M13
6123	L15
6124	L17
6126	N16
6127	N16
6128	M 8
6129	K 3
6130	K 3
6131	K 4
6132	M12
6133	I 12

7.5 Output amplifier section: connection of two or four loudspeakers.

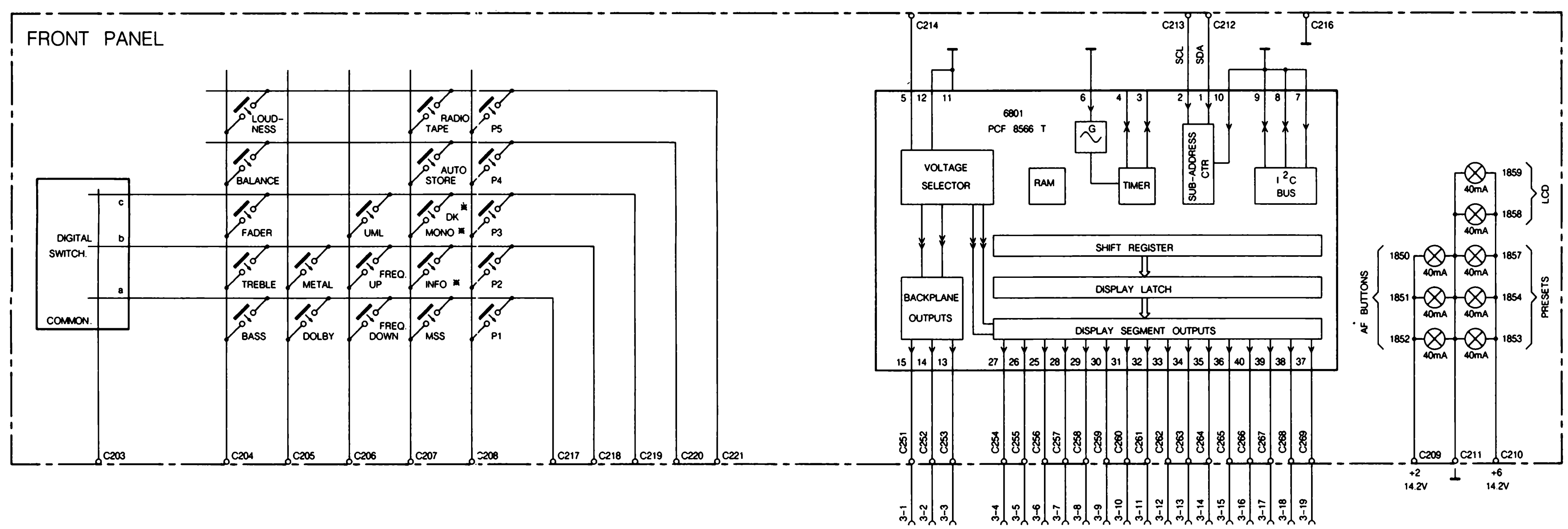
In this chapter we will discuss the switch–over from 4 x 7 W to 2 x 20 W in more detail. The description has been made on the basis of the right–hand channel. To the left–hand channel applies the same story. The assumption is that four loudspeakers are connected. In this case the fader of the SOFAC has to be switched on, which implies that the voltage at pin 9 has to be < 1,5 V (see chapter 7.3). In principle this voltage is coming from one or both outputs (pin 5 and pin 9) of TDA1516Q (6114). If a loudspeaker is connected between B2 and B1 (see Fig. 7.1), el.cap. 2186 will be charged up to the DC voltage level of the amplifier output. In this case this is 6,7 V. For AC voltages the loudspeaker is via 2186 connected to ground. The DC voltage at 2186 is via resistor 3174 fed to pin 9 of the SOFAC so that the fader is active. Now it matters to connect the AF signals of the SOFAC correctly to the output amplifiers. This is done via a differential amplifier (6115 and 6116 for the right–hand channel) whose amplification is one time. The base of 6115 is connected to the right rear (pin 26, R Re) output of the SOFAC. The base of 6116 is via capacitor 2198, which serves for DC voltage decoupling, connected to the right front (pin 25, R Fr) output of the SOFAC. The DC voltage level at the base of 6116 determines which of the two output signals of the SOFAC appears at the common emitters of the transistors. The R Fr signal is via a lowpass filter connected to the inverting input (pin 2) of the TDA1516Q (6114).If four loudspeakers are connected, the R Re signal will have to be applied to the other input of 6114, which implies that 6115 has to be conducting. In the situation shown in Fig. 7.1 this is the case. On the base of 6115 a DC voltage of 3,9 V is present which comes from the output of the SOFAC. If the voltage at the base of 6116 is grater than 3,9 V, this transistor will start conducting. If the base voltage of 6116 becomes less than 3,9 V, it will block while 6115 wil be conducting now.

The R Re signal goes via the base/emitter junction and a lowpass filter to the non–inverting input (pin 13) of the TDA1516Q (6114). Signals R Fr and R Re are in anti–phase now. To correct this the polarity of either of the loudspeakers has to be reversed. Driving the output amplifiers in antiphase is necessary to obtain the 2 x 20 W facility. Below follows a description how the switch–over from 4 x 7 W to 2 x 20 W proceeds. As mentioned before the base voltage of 6116 determines the signal which is set at pin 13 of TDA1516Q (6114).This voltage is switched by 6133. In case 4 x 7 W has been selected, the voltage at el.cap. 2186 will be 6,7 V. This voltage brings via resistor 3173 transistor 6133 in conductance. As a result a current starts to flow through 3173 and 3162. The voltage at their junction which is the result of this current is via 3170 led to the base of 6116. These resistors have been dimensioned so that the base voltage of 6116 is 1,8 V. Now this transistor is blocked while 6115 is conducting so that signals R Fr and R Re are both applied to an input of TDA1516Q (6114). If 2 x 20 W is selected, the connection of B1, B4 to B2 or B3 will be interrupted. Now el.cap. 2186 will discharge across resistor 3163. The result is that the fader of the SOFAC is switched off while transistor 6133 blocks.

The collector of 6133 is floating now causing the base voltage of 6116 to become greater than 3,9 V. The differential amplifier switches over now, which implies that R Re is blocked and R Fr is allowed to pass. Signal R Fr is now connected to the inverting input (pin 2) of one half of 6114 and with the non–inverting input (pin 13) of the other half of 6114. At the outputs (pins 5 and 9) appear the same signals which are in antiphase relative to each other. Between these two outputs the loudspeaker is connected. Because the output voltages at pins 5 and 9 can be added, a greater output power (20 W) is obtained.

Chapter 8. Microcomputer and LCD control

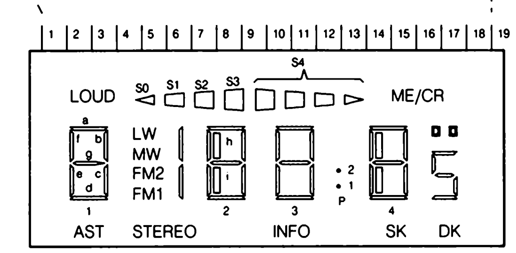
For the sake of completeness the circuit diagrams of the microcomputer (6116) and the EEAROM (6170) are shown in Fig. 8.1. while Fig. 8.2 gives the circuit diagram of the LCD driver and the key matrix. The circuits used are not new but earlier in this description we referred to these diagrams so that they have nevertheless been published in this description as reference. To follow and understand some signal paths these diagrams also are a welcome supplementation.



* ONLY FOR 22DC681/00/50
DELETED: DK, INFO.
ONLY FOR 22DC681/00
ADDED: MONO

L C D PINNING

DISPLAY PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
COMMON A			COM A	L0	A1	B1	S0+S1	LW	S2+S3	F2	A2	B2	S4	A3	B3	F4	A4	B4	ME
COMMON B		COM B		F1	G1	C1	FM2+P2	MW	¦	H2+I2	G2	C2	F3	G3	C3	H4+I4	G4	C4	▯▯
COMMON C	COM C			E1	D1	AS	FM+P1	(FM) 1	ST	E2	D2	IN	E3	D3	SK	E4	D4	DK	5



PRS 02467
T12 812
DC685

Fig.8.2

1162	H 7	2262	H 8	2265	B 8	3217	C 6	3252	D14	3256	B 8	3259	C 5	3263	C14	3266	D 5	3269	D 6	3272	J 3	3275	K 6	3278	I 2	6165	C13	6168	J 8
2260	H13	2263	H 7	2270	J 7	3250	B 8	3253	F13	3257	B10	3260	E13	3264	D 4	3267	D 5	3270	H 6	3273	D13	3276	K 5	3279	I 3	6166	F10	6169	I 7
2261	H13	2264	B 7	2271	J 8	3251	B 9	3255	B 7	3258	B10	3261	E14	3265	D 5	3268	D 6	3271	I 3	3274	D14	3277	H 3	5145	G14	6167	C14	6170	J 4

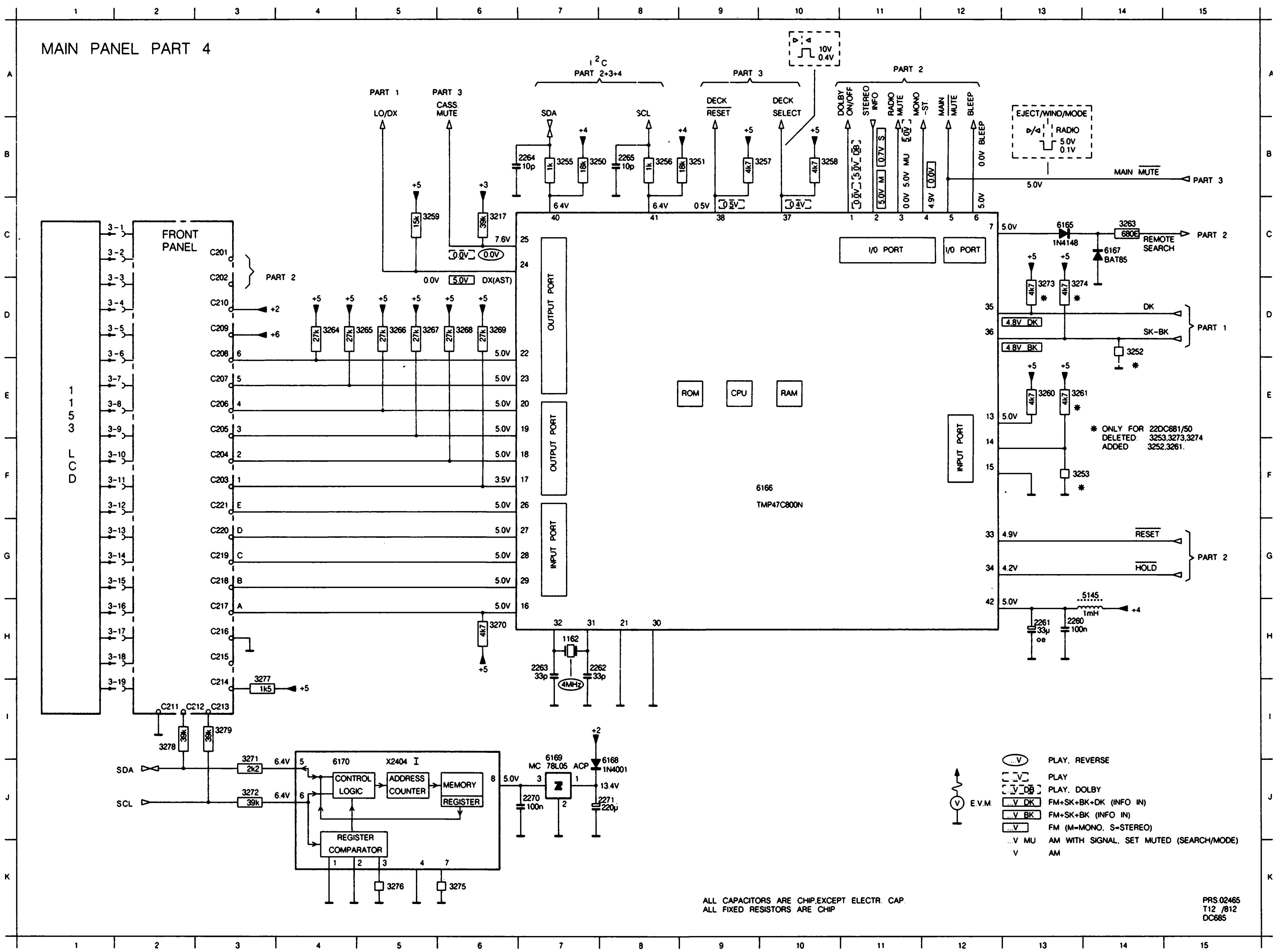


Fig.8.1

NOTES: